

1 WHAT IS CLAIMED IS:

2 1. A method of fabricating a capacitor electrode, comprising:

3 forming an etch stop layer over a surface of an interlayer insulating layer and

4 over a surface of a conductive plug extending at a depth from the surface of the

5 interlayer insulating layer;

6 forming a lower mold layer over the etch stop layer, and adjusting a wet etch

7 rate of the lower mold layer by adding dopants to the lower mold layer during

8 formation of the lower mold layer, and by annealing the lower mold layer;

9 forming an upper mold layer over the surface of the lower mold layer, wherein

10 a wet etch rate of the upper mold layer is less than the adjusted wet etch rate of the

11 lower mold layer;

12 dry etching the upper mold layer, the lower mold layer and the etch stop layer

13 to form an opening therein which exposes at least a portion of the surface of the

14 contact plug;

15 wet etching the upper mold layer and the lower mold layer so as to increase a

16 size of the opening at the lower mold layer and so as to expose a surface portion of

1 the etch stop layer adjacent the surface of the conductive plug; and
2 depositing a conductive material over the surface of the opening in the upper
3 and lower mold layers, the surface portion of the etch stop layer, and an exposed
4 surface of the conductive plug.

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6 2. The method of claim 1, further comprising removing the upper and lower
7 mold layers after depositing the conductive material.

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9 3. The method of claim 1, wherein the lower mold layer is formed of a doped
10 oxide by chemical vapor deposition.

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12 4. The method of claim 3, wherein the lower mold layer is formed of at least
13 one of borophosphosilicate glass (BPSG) and phosphosilicate glass (PSG).

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15 5. The method of claim 1, wherein the upper mold layer is formed of an
16 undoped oxide by plasma enhanced chemical vapor deposition.

1 6. The method of claim 1, wherein the upper mold layer is formed of at least
2 one of plasma-enhanced tetraethylorthosilicate (PE-TEOS), high-density plasma
3 (HDP) oxide, and P-SiH₄ oxide.

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5 7. The method of claim 1, wherein the lower mold layer is formed of
6 borophosphosilicate glass (BPSG), and wherein phosphorous and boron are added
7 to the BPSG prior to said annealing.

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9 8. The method of claim 7, wherein the boron is added in an amount of 2-3
10 wt% of the BPSG, and the phosphorous is added in an amount of 2-3 wt% of the
11 BPSG.

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13 9. The method of claim 1, wherein the lower mold layer is formed of
14 phosphosilicate glass (PSG), and wherein phosphorous is added to the PSG prior to
15 said annealing.

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17 10. The method of claim 9, wherein the phosphorous is added in an amount
18 of less than 5 wt% of the PSG.

1 11. The method of claim 1, further comprising cleaning a surface of the
2 lower mold layer having the adjusted wet etch rate prior to forming the upper mold
3 layer.

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5 12. The method of claim 11, wherein H_2SO_4 is used to clean the surface of
6 the lower mold layer.

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8 13. The method of claim 1, wherein the conductive layer is deposited as a
9 polysilicon by low pressure chemical vapor deposition.

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11 14. The method of claim 1, wherein the upper mold layer and the lower mold
12 layer are wet etch using at least one of SC1 (NH_4OH/H_2O_2 /deionized water) and HF
13 (hydrofluoric acid).

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15 15. The method of claim 1, wherein the etch stop layer is silicon nitride, and
16 the annealing of the lower mold layer is carried out at a temperature of less than

1 700°C.

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3 16. The method of claim 1, wherein the conductive material forms a
4 cylindrical electrode defined by a cylindrical wall and a bottom wall which extends
5 over a surface of the conductive plug, wherein the cylindrical wall extends upwardly
6 from the bottom wall away from the surface of the interlayer insulating layer;

7 wherein the cylindrical wall of the cylindrical electrode is defined by an upper
8 cylindrical wall portion, a lower cylindrical wall portion, and an intermediate cylindrical
9 wall portion located between the upper and lower cylindrical wall portions;

10 wherein a diameter of the upper cylindrical wall portion and a diameter of the
11 lower cylindrical wall portion increase with an increase in a distance from the surface
12 of the bottom wall, wherein a diameter of the intermediate cylindrical wall portions
13 decreases with an increase in a distance away from the surface of the bottom wall,
14 and wherein

15 $A \geq C$, $C > B$, and $C > D$

16 where A is a diameter of the upper cylindrical wall portion at a location farthest

1 from the bottom wall, B is a diameter of the upper cylindrical wall portion at a location
2 nearest to the bottom wall, C is a diameter of the lower cylindrical wall portion at a
3 location farthest from the bottom wall, and D is a diameter of the lower cylindrical
4 wall portion at the bottom wall.

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6 17. A method of fabricating a capacitor, comprising forming a lower
7 electrode over an interlayer insulating layer, forming a dielectric layer over the lower
8 electrode, and forming an upper electrode over the dielectric layer, wherein said
9 forming a lower electrode comprises:

10 forming an etch stop layer over a surface of the interlayer insulating layer and
11 over a surface of a conductive plug extending at a depth from the surface of the
12 interlayer insulating layer;

13 forming a lower mold layer over the etch stop layer, and adjusting a wet etch
14 rate of the lower mold layer by adding dopants to the lower mold layer during
15 formation of the lower mold layer, and by annealing the lower mold layer;

16 forming an upper mold layer over the surface of the lower mold layer, wherein

1 a wet etch rate of the upper mold layer is less than the adjusted wet etch rate of the
2 lower mold layer;

3 dry etching the upper mold layer, the lower mold layer and the etch stop layer
4 to form an opening therein which exposes at least a portion of the surface of the
5 contact plug;

6 wet etching the upper mold layer and the lower mold layer so as to increase a
7 size of the opening at the lower mold layer and so as to expose a surface portion of
8 the etch stop layer adjacent the surface of the conductive plug; and

9 depositing a conductive material over the surface of the opening in the upper
10 and lower mold layers, the surface portion of the etch stop layer, and an exposed
11 surface of the conductive plug.

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13 18. The method of claim 17, wherein said forming a lower electrode further
14 comprises:

15 depositing an insulating layer over the conductive material and within the
16 opening;

1 removing a portion of the insulating layer and the conductive material to
2 expose the upper mold layer; and
3 removing a remaining portion of the insulating layer and the upper and lower
4 mold layers.

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6 19. The method of claim 17, wherein the lower mold layer is formed of a
7 doped oxide by chemical vapor deposition.

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9 20. The method of claim 17, wherein the lower mold layer is formed of at
10 least one of borophosphosilicate glass (BPSG) and phosphosilicate glass (PSG).

11

12 21. The method of claim 17, wherein the upper mold layer is formed of an
13 undoped oxide by plasma enhanced chemical vapor deposition.

14

15 22. The method of claim 17, wherein the upper mold layer is formed of at
16 least one of plasma-enhanced tetraethylorthosilicate (PE-TEOS), high-density

1 plasma (HDP) oxide, and P-SiH₄ oxide.

2
3 23. The method of claim 17, wherein the lower mold layer is formed of
4 borophosphosilicate glass (BPSG), and wherein phosphorous and boron are added
5 to the BPSG prior to said annealing.
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7 24. The method of claim 23, wherein the boron is added in an amount of 2-3
8 wt% of the BPSG, and the phosphorous is added in an amount of 2-3 wt% of the
9 BPSG.
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11 25. The method of claim 17, wherein the lower mold layer is formed of
12 phosphosilicate glass (PSG), and wherein phosphorous is added to the PSG prior to
13 said annealing.
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15 26. The method of claim 25, wherein the phosphorous is added in an
16 amount of less than 5 wt% of the PSG.
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18 27. The method of claim 17, further comprising cleaning a surface of the

1 lower mold layer having the adjusted wet etch rate prior to forming the upper mold
2 layer.

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4 28. The method of claim 27, wherein H_2SO_4 is used to clean the surface of
5 the lower mold layer.

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7 29. The method of claim 17, wherein the conductive layer is deposited as a
8 polysilicon by low pressure chemical vapor deposition.

9

10 30. The method of claim 17, wherein the upper mold layer and the lower
11 mold layer are wet etch using at least one of SC1 (NH_4OH/H_2O_2 /deionized water)
12 and HF (hydrofluoric acid).

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14 31. The method of claim 17, wherein the etch stop layer is silicon nitride,
15 and the annealing of the lower mold layer is carried out at a temperature of less than
16 $700^\circ C$.

1 32. The method of claim 18, wherein the conductiv material forms a
2 cylindrical lower electrode defined by a cylindrical wall and a bottom wall which
3 extends over a surface of the conductive plug, wherein the cylindrical wall extends
4 upwardly from the bottom wall away from the surface of the interlayer insulating
5 layer;

6 wherein the cylindrical wall of the cylindrical lower electrode is defined by an
7 upper cylindrical wall portion, a lower cylindrical wall portion, and an intermediate
8 cylindrical wall portion located between the upper and lower cylindrical wall portions;

9 wherein a diameter of the upper cylindrical wall portion and a diameter of the
10 lower cylindrical wall portion increase with an increase in a distance from the surface
11 of the bottom wall, wherein a diameter of the intermediate cylindrical wall portions
12 decreases with an increase in a distance away from the surface of the bottom wall,
13 and wherein

14 $A \geq C$, $C > B$, and $C > D$

15 where A is a diameter of the upper cylindrical wall portion at a location farthest
16 from the bottom wall, B is a diameter of the upper cylindrical wall portion at a location

1 nearest to the bottom wall, C is a diameter of the lower cylindrical wall portion at a
2 location farthest from the bottom wall, and D is a diameter of the lower cylindrical
3 wall portion at the bottom wall.

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5 33. A capacitor comprising:

6 an interlayer insulating layer having a surface;

7 a conductive plug extending at a depth from the surface of the interlayer

8 insulating layer;

9 an etch stop layer extending over the insulating layer and exposing the

10 conductive plug;

11 a cylindrical lower electrode defined by a cylindrical wall and a bottom wall

12 which extends over a surface of the conductive plug and over a portion of the etch

13 stop layer adjacent the conductive plug, wherein the cylindrical wall extends

14 upwardly from the bottom wall away from the surface of the interlayer insulating

15 layer;

16 a dielectric layer formed over the cylindrical lower electrode; and

1 an upper electrode formed over the dielectric layer;
2 wherein the cylindrical wall of the cylindrical lower electrode is defined by an
3 upper cylindrical wall portion, a lower cylindrical wall portion, and an intermediate
4 cylindrical wall portion located between the upper and lower cylindrical wall portions;
5 wherein a diameter of the upper cylindrical wall portion and a diameter of the
6 lower cylindrical wall portion increase with an increase in a distance from the surface
7 of the bottom wall, wherein a diameter of the intermediate cylindrical wall portions
8 decreases with an increase in a distance away from the surface of the bottom wall,
9 and wherein

$$10 \quad A \geq C, \quad C > B, \quad \text{and} \quad C > D$$

11 where A is a diameter of the upper cylindrical wall portion at a location farthest
12 from the bottom wall, B is a diameter of the upper cylindrical wall portion at a location
13 nearest to the bottom wall, C is a diameter of the lower cylindrical wall portion at a
14 location farthest from the bottom wall, and D is a diameter of the lower cylindrical
15 wall portion at the bottom wall.

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1 34. The capacitor of claim 33, wherein the etch stop film is a silicon nitride

2 film.

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4 35. The capacitor of claim 33, wherein the lower electrode is a polysilicon

5 electrode.

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7 36. The capacitor of claim 33, wherein the dielectric layer is an oxynitride

8 (NO) layer.